REMARKS

Claims 1-4, 6-10, 12-14, 16-19, 21-23, and 25-30 are pending. Claims 1, 3, 9, 13, 18 and 23 have been amended. Claims 5, 11, 15, 20 and 24 have been canceled herein. Support for the amendments is as follows: Claims 1 and 3 incorporate claim 5; claim 9 incorporates claim 11; claim 13 incorporates claim 15; claim 18 incorporates claim 20; and claim 23 incorporates claim 24.

Applicant's Response to the Rejections under 35 USC 103

Claims 1, 2, 13, 15, and 16 stand rejected under 35 USC 103(a) as being unpatentable over ***Nishimura et al.*** (5,736,438) in view of ***Yamazaki et al.*** (5,824,574), and further in view of ***Kawaguchi*** (6,245,622) further in view of ***Yu*** (6,391,695).

Claims 3-8 stand rejected under 35 USC 103(a) as being unpatentable over ***Nishimura et al.*** (5,736,438) in view of ***Yamazaki et al.*** (5,824,574), and further in view of ***Kawaguchi*** (6,245,622) further in view of ***Talwar et al.*** (5,908,307) further in view of ***Yu*** (6,391,695) and ***Noda et al.*** (6,432,802).

Claims 9-12 stand rejected under 35 USC 103(a) as being unpatentable over ***Nishimura et al.*** (5,736,438) in view of ***Yamazaki et al.*** (5,824,574), and further in view of ***Kawaguchi*** (6,245,622) further in view of ***Yu*** (6,391,695) further in view of ***Yoshimi et al.*** (5,698,869).

Claims 18, 20-23, 25 and 26 stand rejected under 35 USC as being unpatentable over ***Nishimura et al.*** (5,736,438) in view of ***Shimizu et al.*** (6,017,781) further in view

of ***Yu*** (6,391,695) further in view of ***Nakajima et al.*** (5,712,191) further in view of ***Yoshimi et al.*** (5,698,869) further in view of ***Noda et al.*** (6,432,802).

In response to the above rejections, Applicant has amended the claims, as detailed above, in order to more distinctly claim the subject matter regarded as the invention. In combination with these amendments, Applicant respectfully traverses. Applicant respectfully submits that the above combinations, even if made, would fail to teach or suggest the presently claimed invention. Specifically, none of the cited references teach or suggest that after a desired region in a semiconductor substrate under a gate electrode is amorphized, the amorphous region is selected to melt.

The Office Action notes that ***Yu*** discloses "required impurities in the amorphous region" (page 3, paragraph 3 of the current Office Action). However, ***Yu*** discloses impurities in an amorphous region to form a back gate region 20 (col. 4, lines 51-53). There is no teaching of the amorphous region for forming a source/drain.

According to the features of the present invention related to currently amended claims 1, 3, 9, 13 and 18, the step of forming a source and drain, after a desired region in a semiconductor substrate under a gate electrode is amorphized, the amorphous region is selected to melt and an impurity extension profile is obtained. As a result, the impurity extension profile shows a sharp difference in concentration and thus makes it possible to provide a controlled method for forming a fine gate.

Although ***Yu*** discloses that ions are implanted into amorphous regions and laser annealing is executed, ***Yu*** fails to disclose or suggest that after a desired region in a

semiconductor substrate under a gate electrode is amorphized, the amorphous region is selected to melt.

Kawaguchi discloses that amorphous regions are silicided. However, ***Kawaguchi*** fails to disclose or suggest that after a desired region in a semiconductor substrate under a gate electrode is amorphized, the amorphous region is selected to melt.

Yamazaki discloses that laser annealing is executed in order to re-crystallize amorphous Si. However, ***Yamazaki*** fails to disclose or suggest that after a desired region in a semiconductor substrate under a gate electrode is amorphized, the amorphous region is selected to melt.

Nishimura discloses that, in re-crystallizing amorphous Si, laser anneal is executed to control a diameter of a crystal. However, ***Nishimura*** fails to disclose or suggest that after a desired region in a semiconductor substrate under a gate electrode is amorphized, the amorphous region is selected to melt.

Applicant therefore respectfully submits that, even if the references are combined, the combination never reaches the feature of the present invention because it fails to disclose or suggest that "after a desired region in a semiconductor substrate under a gate electrode is amorphized, the amorphous region is selected to melt."

For at least the foregoing reasons, it is believed that this application is now in condition for allowance. If, for any reason, it is believed that this application is not in condition for allowance, Examiner is encouraged to contact the Applicants' undersigned attorney at the telephone number below to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully submitted,

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Attachments: Request for Continued Examination w/fee
MJC/SGA/rer